AMENDMENTS TO THE CLAIMS:

1.(currently amended): distortion compensation device, which uses distortion compensation coefficients to subject distortion compensation processing to an input signal and supply the result of the distortion compensation processing to a distorting device, calculates the distortion compensation coefficients based on the input signal before distortion compensation and on the feedback signal fed back from the output side of the distorting device, and stores the calculated distortion compensation coefficients in association with the input signal, comprising:

an AD conversion portion, which AD-converts said feedback signal;

an FFT calculation portion, which performs fast Fourier transform processing of the output of the AD conversion portion, to calculate a spectrum;

a calculation portion, which, based on the FFT calculation results, calculates either the signal-to-noise ratio SNR, or the adjacent channel leakage power ratio ACLR, or the noise level Pn, or the effective number of bits ENOB;

a delay time determination portion, which compares said calculated value at the current time and said calculated value at the immediately preceding time, and based on the comparison result, ~~adjusts~~ delay time of the signal generated in the distorting device and the feedback loop, and repeats the ~~adjustment~~ delay time determination processing to determine said delay time; and,

a delay circuit, in which said delay time is set, and which performs timing adjustment of each of the portions of the distortion compensation device.

2.(original): The distortion compensation device according to claim 1, further comprising a signal synthesis portion which frequency-multiplexes a plurality of transmission signals to generate said input signal.

3.(currently amended): The distortion compensation device according to claim 1, wherein, when the difference in said calculated values is equal to or lower than a set value, said delay time determination portion ends the delay time ~~adjustment~~ determination processing.

4.(currently amended): The distortion compensation device according to claim 3, wherein said delay time determination portion comprises a timer, and performs the delay time determination processing intermittently.

5.(original): The distortion compensation device according to claim 3, wherein, as the difference between said calculated values decreases, said FFT calculation portion increases the number of AD-converted data items for which FFT calculations are performed.

6.(original): The distortion compensation device according to claim 3, comprising a switch to select and supply the output signal of the distorting device to the AD conversion portion when determining the delay time.

7.(original): A distortion compensation device, which uses distortion compensation coefficients to subject distortion compensation processing to an input signal and supply the result of the distortion compensation processing to a distorting device, calculates the distortion

compensation coefficients based on the input signal before distortion compensation and on the feedback signal fed back from the output side of the distorting device, and stores the calculated distortion compensation coefficients in association with the input signal, comprising:

an AD conversion portion, which AD-converts the feedback signal;

an FFT calculation portion, which performs fast Fourier transform processing of the output of the AD conversion portion, to calculate a spectrum;

a calculation portion, which, based on the FFT calculation results, calculates either the signal-to-noise ratio SNR, or the adjacent channel leakage power ratio ACLR, or the noise level Pn, or the effective number of bits ENOB; and,

a clock timing adjustment portion, which compares said calculated value at the current time and said calculated value at the immediately preceding time, and based on the comparison result, adjusts the clock timing of the AD conversion portion.

8.(original): The distortion compensation device according to claim 7, having a signal synthesis portion which frequency-multiplexes a plurality of transmission signals to generate said input signal.

9.(original): The distortion compensation device according to claim 7, wherein said clock timing adjustment portion ends clock timing adjustment when the difference between said calculated values becomes equal to or less than a set value.

10.(original): The distortion compensation device according to claim 9, wherein said clock timing adjustment portion comprises a timer, and performs clock timing adjustment processing intermittently.

11.(original): The distortion compensation device according to claim 9, further comprising a switch which selects and supply the output signal of the distorting device to the AD conversion portion during clock timing adjustment.

12.(original): The distortion compensation device according to claim 7, further comprising:

a delay time determination portion which adjusts the delay time of the signal occurring in the distorting device and feedback loop based on said comparison result and, by repeating the adjustment processing, determines said delay time; and

a delay circuit, in which said delay time is set and which performs timing adjustment of each of the portions of the distortion compensation device,

wherein when the difference between said calculated values becomes equal to or less than a first set value, said delay time determination portion ends delay time determination control, and when the difference between said calculated values becomes equal to or less than a second set value, said clock timing adjustment portion ends clock timing adjustment.

13.(currently amended): A distortion compensation device, which uses distortion compensation coefficients to subject distortion compensation processing to an input signal and supply the result of the distortion compensation processing to a distorting device, calculates the

distortion compensation coefficients based on the input signal before distortion compensation and on the feedback signal fed back from the output side of the distorting device, and stores the calculated distortion compensation coefficients in association with the input signal, comprising:

a band-pass filter, the pass band of which is at least the frequency bands of adjacent channels, and to which is input said feedback signal;

a noise power detection portion, which detects the noise power including the power of adjacent channels from the output of the band-pass filter;

a delay time determination portion, which compares said noise power at the current time with the noise power at the immediately preceding time, ~~adjusts~~ determines the delay time of the signal occurring in the distorting device and feedback loop based on the comparison result, and repeats the ~~adjustment~~ delay time determination processing to determine said delay time; and,

a delay circuit, in which is set said delay time, and which performs timing adjustment in each of the portions of the distortion compensation device.

14.(original): The distortion compensation device according to claim 13, further comprising a signal synthesis portion which frequency-multiplexes a plurality of transmission signals to generate said input signal.

15.(currently amended): The distortion compensation device according to claim 13, wherein said delay time determination portion ends the delay time ~~adjustment~~ determination processing when the difference between said calculated values becomes equal to or less than a set value.

16.(currently amended): The distortion compensation device according to claim 13, wherein said delay time determination portion comprises a timer, and performs the delay time determination processing intermittently.

17.(original): The distortion compensation device according to claim 13, further comprising a switch to select and supply the output signal of the distorting device to the AD conversion portion when adjusting the delay time.